GS1077™
High Availability
CompactPCI System

User’s Guide
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Chapter 1 - Introduction

Welcome to the I-Bus/Phoenix family of CompactPCI computer systems. This manual provides information necessary to set up and maintain the I-Bus/Phoenix GS1077.

The GS1077 System is a High Availability platform designed for markets where maximum “uptime” is required. The GS1077 is designed for 99.999% availability, which equates to 5 minutes maximum downtime per year. The GS1077 system is also designed to meet NEBS Level 3 requirements and has been tested by a certifying lab.

The GS1077 is configured with two Sun UltraSPARC IIi processors running Solaris 7 or 8 and Sun Cluster 2.2. Clustering services minimize down time by allowing applications to fail over to another processor, thereby keeping supported applications running without user intervention. When a failed processor is replaced, the application can be instructed to return to its original functioning state. All critical functions have redundancy, including two sets of mirrored disks in a RAID 0+1 configuration, three N+1 power supplies, and dual network hubs or switches.

Options for the GS1077 include AC or DC power supply inputs, integrated RAID controllers, Telecommunications alarm module, and front pluggable media module with hard drives.

Figure 1-1: GS1077 CompactPCI System
Chapter 1 - Introduction

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Chapter 2 - Specifications

Specifications

D OVERVIEW

The I-Bus/Phoenix GS1077 system is a CompactPCI Platform equipped with two independent system boards (SBCs) configured as a Cluster Server.

It is designed to meet NEBS Level-3 specifications for central office rackmount computer systems.

The GS1077 system accommodates two Sun/SPARC CP1500 SBCs with two independent 7-slot backplanes (GS1077), and the corresponding 80mm rear I/O connectors.

The GS1077 system includes PICMG H.110 compliant backplanes, front pluggable, 300W N+1 redundant power supplies, configurable drive bays for up to eight 5.25" half height drives.

Options include -48VDC power input and RAID controller.

The GS1077 series comes with the Sun Solaris Operating System preinstalled.

Optional Cluster Server Software is available.

Figure 2-1 shows the configuration for GS1077.
Chapter 2 - Specifications

Figure 2-1: GS1077 Configuration

14U
24.5" (622.3 mm)

HOT PLUG FAN TRAY
FILTERED AIR INTAKE

I/O 1  I/O 2  I/O 3  I/O 4  I/O 5  MFR  SYS  SYS  SYS  I/O 8  I/O 9  I/O 10  I/O 11  I/O 12  MFR  SYS  SYS  SYS  P/S 1  P/S 2  P/S 3

5.25 DD  5.25 DD  5.25 DD  5.25 DD  5.25 DD  5.25 DD  5.25 DD  5.25 DD  5.25 DD  5.25 DD  5.25 DD  5.25 DD

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Chapter 2 - Specifications

D MECHANICAL

ENCLOSURE

Designed for EIA RS-310 19" and 24" racks.

Detachable rackmount brackets can be positioned for front flush mount or mid-chassis rackmount.

A separate rackmount bracket design is used for both 19" and 24" racks, both left and right sides, incorporating mounting keyways for temporary hanging of the chassis.

Enclosure front panel incorporates an AC main switch, shrouded to prevent accidental trip, plus LEDs indicating power supply output status.

The front panel can be configured to display a variety of status LEDs (up to 30).

Backplane cooling fans are hot pluggable via a single tray.

Cool air intake incorporates a user removable, washable filter element.

main input and circuit breaker are on the rear of the enclosure.

Provision is made for additional, optional telephony voltage inputs at the rear of the enclosure.

BASIC CHASSIS CONFIGURATION

Eurocard 6U card cage, per PICMG 2.0 Rev 3.0, CompactPCI specification.

Space for a total of 14 CompactPCI slots plus three 8HP power supplies.

Total rack height is 14U (24.50"/622.3mm) with upper drive bay.

Cool air intake is in front below the backplane card cage.

Hot air exhaust is in the rear above the 6U backplane.

Overall dimensions are 24.50" High, 17.00" Wide, 12.00" deep.
Chapter 2 - Specifications

UPPER DRIVE BAY
Mounts eight 5.25” half height drives vertically.
Drive shuttles are used allowing the drives to be mounted or replaced without dismounting the enclosure from the rack.
Mounts up to four exhaust fans on a rear hot-plug bracket.
Drive cooling air is filtered at intake; filter is user removable and washable.

POWER SUBSYSTEM
N+1 redundant power supplies, delivering up to 600W throughput from AC or DC main input.
Forced current sharing for +5V, +3.3V and +12V; diodes are internal to the pluggable supply.
AC input range: 90-264VAC, 47-63Hz, auto sensing, auto ranging.
DC input range: -40 to –72VDC.
Internal Power Factor Correction (PFC) to meet IEC EN61000-3 requirements for harmonic distortion and flicker.

PLUGGABLE SUPPLY
Maximum loads: +5VDC @ 30A  +3.3VDC @ 45A  +12VDC @ 12A  -12VDC @ 3A; combined total output not to exceed 300W; combined total output of +5V and +3.3V not to exceed 200W.
No minimum loads required for normal operation.
Ripple: 50mV for +5V and 3.3V, 100mV for +12V and –12V.
Load regulation: ±2% for +5V, +3.3V and +12V; ±5% for –12V.
Line regulation: ±0.5% for all outputs.
MTBF: 100,000 hrs, full load at 25°C (MIL-217).
Capable of delivering full rated loads at system operating ambient temperature with 400 LFM through the supply.
Size: CompactPCI 6U X 8HP (1.6” wide).
Interface connector: Positronics PCI38M400A1, mate on power backplane is Positronics PCI38F300A1.
Chapter 2 - Specifications

POWER BACKPLANE

Accepts up to three pluggable supplies.

Input power connector: AMP 350715-1, pin 1 chassis ground, pin 2 AC line, pin 3 AC neutral.

DC output: 8 headers, Molex 39-28-1203; also individual M4 screw terminals, rated 25A; 4 for +5V, 5 for +3.3V, 1 each for +12V and –12V, and 10 for DC return.

Size: 11.10” high, 4.80” wide.

HARDWARE

CPU BOARD

The system consists of two SBCs in a single system. The various network and SCSI cards are duplicated on each SBC unit. An external 10/100BaseT Ethernet Hub is also part of the system.

<table>
<thead>
<tr>
<th>Model</th>
<th>SBC/RTM</th>
<th>Multi Function I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>GS1077</td>
<td>SUN – CP1500 SPARCengine 360MHz CPU 128 (512) MB RAM.</td>
<td>IntraServer ITI-8241C-S. Dual SCSI and quad Ethernet card with integrated video port.</td>
</tr>
<tr>
<td></td>
<td>Active Transition card SUN XCP-TRN CPCI I/O for CP1500 SCSI, serial ports, PS/2 keyboard, mouse, floppy, parallel port.</td>
<td>IntraServer ITI-8241C-R rear transition card for ITI-8241C-S.</td>
</tr>
</tbody>
</table>

The following is provided by the Multi-Function I/O (MFIO) board:

- Dual Ultra2/LVD for 80 MB/sec bandwidth capability.
- Status lights on both SCSI channels for termination, SCSI bus activity, and LVD speed indicator.
- Four independent Ethernet channels for High Availability Network Support and Sun Trunking Software.
- Video adapter with 4 MB VRAM (for GS1077 – SUN-based system).
- Sixty-four bit CompactPCI interface.
- Rear I/O module.
- ClusterReady technology for clustering and fail-over capability.
Chapter 2 - Specifications

CompactPCI BACKPLANE
PICMG 2.0 Rev 2.1, PICMG 2.1 Rev 1.0 Hot Swap compliant, and PICMG 2.1 Rev 1.0 computer telephony compliant backplane modules are used as the system backplane.
GS1077 backplane consists of two independent 7-slot CompactPCI backplane modules.
A separate power supply backplane is used to accept up to three pluggable power supply modules.
Power is connected to each CompactPCI Backplane Module through a power cable assembly.

SOFTWARE
The system is preloaded with Solaris 7 or 8 operating system.
Sun Cluster 2.2 software is optional

ENVIRONMENTAL
TEMPERATURE
Operating temp 0°C to 40°C.
Short-term operating temp –5°C to 55°C.
Non-operating temp –40°C to 70°C.
HUMIDITY
Operating humidity 5-85% @ 40°C (non-condensing).
Non-operating humidity 0-95% @ 40°C (non-condensing).
ALTITUDE
Operating altitude 6000 ft. at operating temp, 15,000 ft. at derated temp.
Non-operating altitude 40,000 ft.
VIBRATION/SHOCK
Operating vibration 0.25g @ 2-100 Hz, 1.5g @ 100-500 Hz.
Storage/transport vibration 2g @ 5-500 Hz.
Operating shock 10g @ 11 msec, and NEBS earthquake zone 4.
Storage/transport shock 30g @ 11 msec.
Chapter 2 - Specifications

D SAFETY AGENCY
UL 1950, Recognized Component.
cUL or CSA 950 Approved.
TUV EN 60950 Certified.
CE Certified.
FCC Class A.

D CLUSTER SERVER OPERATION
The objective of clustering is to provide very high levels of application and data availability. Cluster service minimizes downtime and reduces IT costs by providing an architecture that keeps systems running in the event of a single system failure.

During normal operation, one SBC will be active while the other will be in a stand-by mode. The network interconnection between the two SBCs, in conjunction with the cluster server software running on them allows each SBC to monitor the health of the other SBC in the system, thus providing a fail-over and fail-back capability of the system.

Cluster Server Software will be run on each of the SBCs to support a high-availability system. The key cluster service features include:

- Automatically detects and recovers from a failed SBC.
- Support for system upgrades while in full operation.
- Health monitoring of standard applications and servers.
- Plug and Play support for networks and disks.

G CLUSTER SERVER ARCHITECTURE
Figure 2 shows a block diagram for the Cluster Server System. Client accesses the cluster system from the Network (LAN, Internet, etc.), and sees a system with a single processing module.

Internally, there are two independent SBCs, a LEFT and a RIGHT System, that are connected together through redundant ethernet links, Hme0 and Qfe0, allowing one system to monitor the activities of the other system. For the sake of this explanation, the LEFT System is pre-configured be the monitoring system.
After the boot-up process is completed, the LEFT System will start sending sanity check packet to the RIGHT System through the heart-beat ethernet link, Hme0. The RIGHT System is used to run the actual software (eg. a database application).

Figure 2-2. Cluster Server System Configuration
Chapter 2 - Specifications

In response to the sanity check packet sent from the LEFT System, the RIGHT System will have to send a reply packet indicating that it is functioning properly. In the case that the reply packet is not received within a certain time frame, the LEFT System may react by declaring the RIGHT System as not functioning anymore, and decide to take over the processing of the RIGHT System.

The actual implementation of fail-over may be more complicated with the availability of a second heart-beat ethernet link, Qfe0.

The Hard Disk array consists of a mirrored disk array with two physical disks each. Each of the two hard disks in the mirrored configuration will be connected to independent SCSI ports (scsi1 and scsi2).

The two SCSI ports provide redundancy as files are written concurrently to both mirror sides of the array. Two physical drives controlled by one SCSI port allows doubling of access speed to the drives.

The drives are mounted in the software to one system at a time (LEFT or RIGHT). The system that takes over the processing when one side fails will mount its drives and therefore has access to the same physical drives used by the failed system.

The heart-beat link will be used further for kernel-to-kernel level query of the other system's processes. This way the stand-by system is aware of what the other system is running and can perform a relatively quick system switch in the case of a fail-over.

The client communication link to the system is redundant with two independent ethernet links (Qfe1 and Qfe2) connected to the MFIO board.
This chapter discusses the removal and installation of the CPU board module, add-in board modules, rear I/O modules, backplane, fan tray, system fans, and air filter.

**CAUTION!**

Unless working on hot-swap components, always shut down the system and turn OFF all power and disconnect the power cord before working on the system.

**CAUTION!**

Electrostatic discharge (ESD) may damage memory chips, programmed devices, and other electrical components. ESD can be prevented by wearing a wrist strap attached to a ground post on a static mat.

**CAUTION!**

Connector pins on CompactPCI backplanes are extremely delicate and can easily be bent. Precise alignment and proper insertion/ejection procedures are critical in order to avoid bending backplane pins.

**CPU Board**

The Sun SPARCengine CP1500 CPU modules are mounted through the front of the enclosure. Each is held in place with two injector/ejector handles that stabilize the board when they are engaged. They are also secured by two captive screws located on the CPU board module’s faceplate. See the following instructions if the CPU module needs to be removed for maintenance or replacement.

**Removal and installation of the CPU board module**

1. Shut down the system and turn off the main system power.
2. Place the chassis on an ESD-safe work surface.
3. Loosen the two screws on the CPU board module’s faceplate. Note: When loosened, the screws should be pushed inward to prevent obstructing the movement of the injector/ejector handles.
Chapter 3 - Hardware

4 Completely retract the injector/ejector handles by pressing them away from each other.
   Note: Some force may be required.

5 Slide the CPU board module out of the chassis.

6 Using the module guides, slide the new CPU board into the chassis, making sure to align the two guide pins with the round holes in the card guides inside the chassis.

7 Engage the injector/ejector handles by pressing them towards each other.
   Note: Again, some force may be required.

8 Secure the CPU board module by tightening the two captive screws.
Chapter 3 - Hardware

Multi-Function I/O Boards

CAUTION!

Unless working on hot-swap components, always shut down the system and turn OFF all power and disconnect the power cord before working on the system.

CAUTION!

Electrostatic discharge (ESD) may damage memory chips, programmed devices, and other electrical components. ESD can be prevented by wearing a wrist strap attached to a ground post on a static mat.

CAUTION!

Connector pins on CompactPCI backplanes are extremely delicate and can easily be bent. Precise alignment and proper insertion/ejection procedures are critical in order to avoid bending backplane pins.

In this cluster system, an IntraServer Multi-Function I/O (MFIO) board operates in conjunction with each of the two CP1500 CPU boards. The MFIO board provides the communication function between the active CPU board and the monitoring CPU board.

All MFIO board modules are mounted through the front of the enclosure. They are held in place with two injector/ejector handles that stabilize the boards when they are engaged.

The GS1077 provides for full hot swap capability of MFIO boards. The following steps should be taken to remove and install add-in boards.

1. Choose which card is to be hot swapped.
2. Toggle the bottom injector/ejector handle of the card down or activate the hot swap thumb switch.
3. The card’s blue LED should light, indicating that the card is safe to remove.
4. Remove the card as normal.
Chapter 3 - Hardware

To insert or re-insert a card back into that slot, the following must be done.

1. Insert the card.

2. The blue LED will light momentarily and should diminish after full insertion is complete.

3. The operating system should recognize the card and accomplish the correct steps to allocate resources and load drivers.

Figure 3-2: Multi-Function I/O Board
Add-in boards

CAUTION!

Unless working on hot-swap components, always shut down the system and turn OFF all power and disconnect the power cord before working on the system.

CAUTION!

Electrostatic discharge (ESD) may damage memory chips, programmed devices, and other electrical components. ESD can be prevented by wearing a wrist strap attached to a ground post on a static mat.

CAUTION!

Connector pins on CompactPCI backplanes are extremely delicate and can easily be bent. Precise alignment and proper insertion/ejection procedures are critical in order to avoid bending backplane pins.

All add-in board modules are mounted through the front of the enclosure. They are held in place with two injector/ejector handles that stabilize the boards when they are engaged.

The GS1077 provides for full hot swap capability of add-in boards, providing the operating system is Full Hot Swap compliant and the add-in boards are designed for Hot Swap capability. The following steps should be taken to remove and install add-in boards:

1. Choose which card is to be hot swapped.
2. Toggle the bottom injector/ejector handle of the card down or activate the hot swap thumb switch.
3. The card's blue LED should light, indicating that the card is safe to remove.
4. Remove the card as normal.
Chapter 3 - Hardware

To insert or re-insert a card back into that slot, the following must be done.

1 Insert the card.

2 The blue LED will light momentarily and should diminish after full insertion is complete.

3 The operating system should recognize the card and accomplish the correct steps to allocate resources and load drivers.

For hot swap instructions on other third party hot swap software, consult the applicable instruction manual for the software.

Removal and installation of non-hot swap add-in boards for systems without hot swap software installed:

1 Shut down the system and turn off the main system power.

2 Place the chassis on an ESD-safe work surface.

3 Loosen the screws on the add-in board’s faceplate, if any.

4 Completely retract the injector/ejector handles of the add-in board module by pressing them away from each other.
   Note: Some force may be required.

5 Slide the add-in board module out of the chassis.

6 Using the module guides, slide the new add-in board into the chassis, making sure to align the two guide pins with the round holes in the card guides inside the chassis.

7 Engage the injector/ejector handles by pressing them towards each other.
   Note: Again, some force may be required.

Note: If you do not plan on immediately replacing a removed add-in board, you must close the space left open with a filler panel in order to maintain EMI specifications.
Chapter 3 - Hardware

Rear I/O Transition Modules

CAUTION!

Unless working on hot-swap components, always shut down the system and turn OFF all power and disconnect the power cord before working on the system.

CAUTION!

Electrostatic discharge (ESD) may damage memory chips, programmed devices, and other electrical components. ESD can be prevented by wearing a wrist strap attached to a ground post on a static mat.

CAUTION!

Connector pins on CompactPCI backplanes are extremely delicate and can easily be bent. Precise alignment and proper insertion/ejection procedures are critical in order to avoid bending backplane pins.

The GS1077 is configured to support rear I/O transition modules. As an optional feature, the CP1500 rear transition module may be installed.

Please note, however, that because of space requirements for SCSI cabling for the rear transition board in slot #7, rear transition slot #8 is covered by a filler panel and is not usable for a rear I/O transition module.

To remove and reinstall the rear I/O module from slot #7:

1. Shut down the system and turn off the main system power.
2. Place the chassis on an ESD-safe work surface
3. Remove the filler panel from slot #8.
4. Loosen the two screws on the rear I/O module’s faceplate as much as possible.

Note: The screws are captive to the faceplate and cannot be completely removed. (Note: some modules may not have screws on the faceplate).
Chapter 3 - Hardware

5 Completely retract the injector/ejector handles by pressing them away from each other.

Note: This may require some force.

6 Slide the rear I/O module out of the chassis just enough to unplug the SCSI cable connector. Then complete the removal of the module.

7 Using the module guides, start to slide the new rear I/O module into the chassis, making sure to align the two guide pins with the round holes in the card guides inside the chassis.

8 Before completing the insertion, plug the SCSI cable connector into its mating connector on the board. Then fully insert the board module.

9 Engage the injector/ejector handles by pressing them towards each other.

Note: Again, some force may be required.

Removal and installation of other rear I/O modules:

1 Shut down the system and turn off the main system power.

2 Place the chassis on an ESD-safe work surface.

3 Loosen the two screws on the rear I/O module's faceplate as much as possible.

Note: The screws are captive to the faceplate and cannot be completely removed. (Note: some modules may not have screws on the faceplate).

4 Completely retract the injector/ejector handles by pressing them away from each other.

Note: This may require some force.

5 Slide the rear I/O module out of the chassis.

6 Using the module guides, slide the new rear I/O module into the chassis, making sure to align the two guide pins with the round holes in the card guides inside the chassis.

7 Engage the injector/ejector handles by pressing them towards each other.

Note: Again, some force may be required.

8 Secure the rear I/O module by tightening the two faceplate screws if they are present.
Chapter 3 - Hardware

Note: If you do not plan on immediately replacing a removed I/O module, you must close the space left open with a filler panel in order to maintain EMI specifications.

9 Turn on the main system power.

![CP1500 Rear I/O Transition Module](image)

Figure 3-3: CP1500 Rear I/O Transition Module

**Backplane**

Backplane Connector Pin Assignments

The GS1077 supports two 7-slot CompactPCI backplanes, accessible by removing the top of the chassis. See Appendix 1, Tables A1-1 thru A1-5 for connector information for the CompactPCI backplane.
Chapter 3 - Hardware

Backplane Configuration

On the rear of the backplane at the top of each slot there is a set of 5 jumpers that set the slot’s geographic address. The geographic address should be set so that (as viewed from the front) the leftmost slot in the system has geographic address “1,” and the address increments by 1 for each slot to the right up to 7. Thus, for the GS1077, each of the two system slots (slots #7 and #14) have geographic addresses of “7” since each backplane comprises a separate system.

Each backplane also has one additional set of 5 jumpers, identified as JP11, that set the backplane’s shelf address. This set is located between two of the slots near the top of the backplane and is an optional feature to identify a specific system in a rack of many systems.

Table A1-6 in Appendix 1 shows how to set the geographic and shelf address jumpers. The pin numbers refer to the pins in the 2x5 set of jumpers at the top of each slot.

In addition, the backplane has jumpers for clock routing, reset and voltage sensing. Table A1-7 gives these settings for each 7-slot backplane.

Figure 3-4 shows the location of the various jumpers on each of the backplanes.

Do not attempt to remove the backplanes from the chassis. Except for the settings described above, the backplane is not a user serviceable item. Please contact I-Bus/Phoenix Technical Support for further information.
Figure 3-4: Jumper Location 7-Slot Backplane Segment
Chapter 3 - Hardware

Fan Plenum and Chassis Fan

Figure 3-5: Fan Tray
(partially withdrawn)

Removal and installation of the hot-swap fan tray

Note: Removing the fan tray interrupts power to all chassis fans. As a result, you should have another fan tray ready to install immediately after the first one is removed to prevent the unit from overheating.

1. Loosen the two captive thumb screws located on either side of the fan access door at the front of the enclosure.
2. Open the access door.
3. Slide the fan tray out of the chassis.
4 Carefully align the right and left hand edges of the fan tray with their guide slots in the chassis and slide the replacement fan tray into the chassis and press firmly to engage the power connectors at the rear of the chassis. If the system is energized and the tray is correctly aligned, the fans will immediately start running as contact is made with the rear power connectors.

5 Close the access door and tighten the two captive thumb screws.

Removing/installing a fan

1 Remove the fan tray.

2 Remove the screws securing the fan and its two finger guards to the fan tray, taking care not to lose any of the flat washers.

3 Swap out the old fan for a new one and place it between the two finger guards.

Note: The arrow indicating the fan air direction.

4 Orient finger guard mounting spokes toward the fan.

5 Secure the new fan and the finger guards to the fan tray using the same screws and flat washers removed in step 2.

Note: The washer goes between the finger guard and the fan tray.

6 Install the fan tray in the chassis.

![Figure 3-6: Fan Subassembly](image)
Chapter 3 - Hardware

Chassis Filters

Using a vacuum cleaner or compressed air, clean the chassis filters once a month or whenever dust accumulates on them. Failure to do so will cause the unit to overheat and fail.

Removing/Installing the chassis filters

1. Loosen the two captive thumb screws located on either side of the fan access door at the front of the chassis.
2. Open the access door.
3. Remove the filter from the filter plate and clean it.
4. Replace the filter in the filter plate and completely close the fan access door.

Note: This may require some force.
5. Secure it with the captive thumb screws.
Chapter 4 - Power Distribution

This chapter discusses the power supply, power switch, and input circuit breaker, and provides installation and removal instructions for each.

CAUTION!

Unless working with hot-swap components, always shut down the system, turn OFF all power, and disconnect the power cords before working on the system.

Power Supplies

Chassis DC power is provided by three 300W AC input hot swap, current sharing power supplies in an N+1 configuration. One of the power supplies may be removed and replaced with the system power on without interrupting the system, provided the remaining supplies are sufficient to power all of the CPU, drives and add-in cards installed in the system.

Removing and installing the power supply module

1. Loosen the two screws on the power supply module’s faceplate as much as possible.

   Note: The screws are captive to the faceplate and cannot be completely removed.

2. Completely retract the injector/ejector handles by pressing them away from each other.

   Note: This may require some force.

3. Slide the power supply module out of the chassis.

4. Slide the replacement power supply module into the chassis, making sure to align the guide pins to their card guides.

5. Engage the injector/ejector handles by pressing them toward each other.

6. Secure the power supply module by tightening the two faceplate screws.
Chapter 4 - Power Distribution

**Input Circuit Breaker**

The following instructions apply to all input circuit breakers.

The main power switch is an input circuit breaker located on the rear panel. However, the front panel switch can be used to power down the unit. This switch is wired in series with the rear panel circuit breaker. To avoid shock hazard, turn off both the power supply switch and the circuit breaker.

**Removing/Replacing the input circuit breaker**

1. Shut down the system and turn off the main system power.
2. Disconnect the power cord/cable.
3. Remove the four screws that mount the breaker plate to the rear panel.
4. Gently pull the breaker plate away from the rear panel until the circuit breaker and the quick-disconnect terminals can be easily accessed.
5. With the wires still connected, squeeze the spring clips on the sides of the old circuit breaker, pushing it through the front of the breaker plate until it pops out the front of the plate.
6. Remove the wires, one by one from the old circuit breaker, and attach each one to the new circuit breaker as it is removed from the old breaker, placing it on the correct terminal.
7. Push the new circuit breaker back into position in the breaker plate until the spring clips on the breakers side snap into place.
8. Re-install the plate.
9. Plug in the power cord or reinstall the power cable.
10. Turn the power on.
Chapter 5 - Drive Bay

This chapter describes the removal and installation of the drives.

Removing/installing the drives

For the Eight Drive Bay

**Note:** The following instructions assume the drives are not mounted in removable drive shuttles. If they are in shuttles, refer to the shuttle manufacturer’s product manual for proper removal/installation instructions.

1. Shut down the system and turn off the main system power. If the system is rack mounted, remove it from the rack.

2. Remove the drive fan tray by loosening the thumb screws on either end of the bracket.

3. Disconnect the power and interface cables from all drives.

Figure 5-2: Eight Drive Bay
(Hard Drives Mounted in Shuttles)
Chapter 5 - Drive Bay

4 Remove the drive module from the chassis top by removing the six screws from each side panel and lifting it off the chassis. Be careful of the serrated metal gasketing. It is delicate and easily damaged, and it is sharp.

5 Disconnect the cables to the front panel power switch and display circuit board assembly.

6 Place the drive module on its side on another ESD safe work surface. Open the drive filter door.

7 Remove the four mounting screws holding the desired drive to the module. Be sure to save the flat washers and insulating grommets (if applicable).

8 Mount the replacement drive using the hardware removed in step 7 above. Be sure to replace the insulating grommets and flat washers if applicable.

9 Carefully place the drive module on top of the chassis, replugging the cables to front panel components.

10 Insert and tighten the six screws on each side panel.

11 Reconnect all drive power and interface cables.

12 Replace and secure the drive fan tray. Close and secure the drive filter door.

13 Turn the power on.
Chapter 6 - Software

Software

The GS1077 is preloaded with Sun Solaris 7 or 8 Operating System. For software configuration support on this platform, refer to the software manufacturer’s Installation and Configuration manual.

Sun Cluster 2.2 software is optional.
Chapter 6 - Software

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## P1 Connector Pin Assignments (System Slot)

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<td>VCC</td>
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<td>GND</td>
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<td>PAR</td>
<td>C/BE[1]</td>
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<td>LOCK_</td>
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<td>TRDY_</td>
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<td>Key 12-14</td>
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Table A1-1: P1 Connector Pin Assignments (System Slot)
# Appendix 1 - Technical Reference

## P1 Connector Pin Assignments (I/O Slot)

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<tr>
<th>Pin #</th>
<th>Z</th>
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<td>STOP_</td>
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**Key**

12-14

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Table A1-2: P1 Connector Pin Assignments (I/O Slot)
Appendix 1 - Technical Reference

P1 Signal Descriptions

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### Appendix 1 - Technical Reference

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_ = signal is active low
* = signal is not currently used

Table A1-3: P2 Connector Pin Assignments (System Slot)
## Appendix 1 - Technical Reference

### P2 Connector Pin Assignments (I/O Slot)

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<td>GND</td>
<td>RSV*</td>
<td>RSV*</td>
<td>RSV*</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>BRSVP2A18</td>
<td>BRSVP2B18</td>
<td>BRSVP2C18</td>
<td>GND</td>
<td>BRSVP2E18</td>
<td>GND</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>BRSVP2A17</td>
<td>GND</td>
<td>RSV*</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>BRSVP2A16</td>
<td>BRSVP2B16</td>
<td>RSV*</td>
<td>GND</td>
<td>BRSVP2E16</td>
<td>GND</td>
</tr>
<tr>
<td>15</td>
<td>GND</td>
<td>BRSVP2A15</td>
<td>GND</td>
<td>RSV*</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>14</td>
<td>GND</td>
<td>AD[35]</td>
<td>AD[34]</td>
<td>AD[33]</td>
<td>GND</td>
<td>AD[32]</td>
<td>GND</td>
</tr>
<tr>
<td>13</td>
<td>GND</td>
<td>AD[38]</td>
<td>GND</td>
<td>V(I/O)</td>
<td>AD[37]</td>
<td>AD[36]</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>AD[52]</td>
<td>GND</td>
<td>V(I/O)</td>
<td>AD[51]</td>
<td>AD[50]</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>AD[56]</td>
<td>AD[55]</td>
<td>AD[54]</td>
<td>GND</td>
<td>AD[53]</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>AD[59]</td>
<td>GND</td>
<td>V(I/O)</td>
<td>AD[58]</td>
<td>AD[57]</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>RSV*</td>
<td>GND</td>
<td>RSV*</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>RSV*</td>
<td>RSV*</td>
<td>UNC</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>1</td>
<td>GND</td>
<td>RSV*</td>
<td>GND</td>
<td>RSV*</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
</tbody>
</table>

_= signal is active low
"= signal is not currently used

Table A1-4: P2 Connector Pin Assignments (I/O Slot)
## Appendix 1 - Technical Reference

### P2 Signal Descriptions

<table>
<thead>
<tr>
<th>General</th>
<th>V(I/O)</th>
<th>5V or 3.3V power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>GND</td>
<td>To digital ground plane</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PCI Bus Signals (64-bit extension)</th>
<th>AD(32:63)</th>
<th>Address/Data bus</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>C/BE(4:7)</td>
<td>Command/Byte Enable bus</td>
</tr>
<tr>
<td></td>
<td>PAR64</td>
<td>64-bit Bus parity</td>
</tr>
<tr>
<td></td>
<td>BRSVPxxx</td>
<td>PCI bus reserved signals</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PCI bus arbitration signals</th>
<th>GNT(6:1)</th>
<th>Bus grants</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>REQ(6:1)</td>
<td>Bus requests</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PCI bus clocks</th>
<th>CLK(6:1)</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Miscellaneous signals</th>
<th>PRST</th>
<th>Push Button Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>DEG</td>
<td>Degrade signal (Power Supply)</td>
</tr>
<tr>
<td></td>
<td>FAL</td>
<td>Supply Fail Signal (Power Supply)</td>
</tr>
<tr>
<td></td>
<td>GA(4:0)</td>
<td>Geographic Addressing</td>
</tr>
<tr>
<td></td>
<td>SYSEN</td>
<td>System slot identification (Grounded at the system slot)</td>
</tr>
<tr>
<td></td>
<td>64EN</td>
<td>64-bit bus enable</td>
</tr>
</tbody>
</table>

### P3, P4, P5 Connectors Pin Assignments (System Slot)

P3, P4, and P5 are used for the purpose of providing access to the rear I/O. There is no connection on the backplane to these connectors at the system slot. The P3, P4, and P5 connector pinouts are unique to the CP1500 SPARC CPU board and described in the SPARCengine CP1500 360MHz/440MHz Technical Reference and Manual, located at the SPARC web site: [http://www.sun.com/microelectronics/SPARCengineCP/1500](http://www.sun.com/microelectronics/SPARCengineCP/1500)
## Appendix 1 - Technical Reference

### P4 Connector Pin Assignments (Computer Telephony Bus) (I/O Slot)

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>NP</td>
<td>SGA4</td>
<td>SGA3</td>
<td>SGA2</td>
<td>SGA1</td>
<td>SGA0</td>
<td>FG</td>
</tr>
<tr>
<td>24</td>
<td>NP</td>
<td>GA4</td>
<td>GA3</td>
<td>GA2</td>
<td>GA1</td>
<td>GA0</td>
<td>FG</td>
</tr>
<tr>
<td>23</td>
<td>NP</td>
<td>+12V</td>
<td>CT_Reset_</td>
<td>CT_EN_</td>
<td>-12V</td>
<td>CT_MC</td>
<td>FG</td>
</tr>
<tr>
<td>22</td>
<td>NP</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>FG</td>
</tr>
<tr>
<td>21</td>
<td>NP</td>
<td>-SELVbat</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>SELVBatRtn</td>
<td>FG</td>
</tr>
<tr>
<td>20</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
</tr>
<tr>
<td>19</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>SELVBatRtn</td>
<td>NP</td>
</tr>
<tr>
<td>18</td>
<td>NP</td>
<td>VRG</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
</tr>
<tr>
<td>17</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
</tr>
<tr>
<td>16</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
</tr>
<tr>
<td>15</td>
<td>NP</td>
<td>-Vbat</td>
<td>NP</td>
<td>NP</td>
<td>NP</td>
<td>VBatRtn</td>
<td>NP</td>
</tr>
</tbody>
</table>

Key 12-14

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>NP</td>
<td>CT_D29</td>
<td>CT_D30</td>
<td>CT_D31</td>
<td>V(I/O)</td>
<td>CT_FRAME_A_</td>
<td>GND</td>
</tr>
<tr>
<td>10</td>
<td>NP</td>
<td>CT_D27</td>
<td>VCC3</td>
<td>CT_D28</td>
<td>VCC</td>
<td>CT_FRAME_B_</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>NP</td>
<td>CT_D24</td>
<td>CT_D25</td>
<td>CT_D25</td>
<td>GND</td>
<td>FR_COMP_</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>NP</td>
<td>CT_D21</td>
<td>CT_D22</td>
<td>CT_D23</td>
<td>VCC</td>
<td>CT_C8_A</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>NP</td>
<td>CT_D19</td>
<td>VCC</td>
<td>CT_D20</td>
<td>GND</td>
<td>CT_C8_B</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>NP</td>
<td>CT_D16</td>
<td>CT_D17</td>
<td>CT_D18</td>
<td>GND</td>
<td>CT_NETREF_1</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>NP</td>
<td>CT_D13</td>
<td>CT_D14</td>
<td>CT_D15</td>
<td>VCC3</td>
<td>CT_NETREF_2</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>NP</td>
<td>CT_D11</td>
<td>VCC</td>
<td>CT_D12</td>
<td>VCC3</td>
<td>SCLK</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>NP</td>
<td>CT_D8</td>
<td>CT_D9</td>
<td>CT_D10</td>
<td>GND</td>
<td>SCLKx2</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>NP</td>
<td>CT_D4</td>
<td>CT_D5</td>
<td>CT_D6</td>
<td>CT_D7</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>1</td>
<td>NP</td>
<td>CT_D0</td>
<td>VCC3</td>
<td>CT_D1</td>
<td>CT_D2</td>
<td>CT_D3</td>
<td>GND</td>
</tr>
</tbody>
</table>

_ = signal is active low

Table A1-5: P4 Connector Pin Assignments (Computer Telephony Bus) (I/O Slot)
# Appendix 1 - Technical Reference

## P4 Signal Descriptions (Computer Telephony Bus)(I/O Slot)

### General

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>5V power</td>
</tr>
<tr>
<td>VCC3</td>
<td>3.3V power</td>
</tr>
<tr>
<td>V(I/O)</td>
<td>5V or 3.3V power</td>
</tr>
<tr>
<td>+12V</td>
<td>12V power</td>
</tr>
<tr>
<td>-12V</td>
<td>-12V power</td>
</tr>
<tr>
<td>GND</td>
<td>To digital signal ground plane</td>
</tr>
<tr>
<td>FG</td>
<td>To chassis (frame) ground</td>
</tr>
<tr>
<td>SGA(4:0)</td>
<td>Shelf enumeration bus signals</td>
</tr>
<tr>
<td>GA(4:0)</td>
<td>Slot ID signals; not bussed</td>
</tr>
<tr>
<td>RSV</td>
<td>Reserved pin</td>
</tr>
<tr>
<td>NP</td>
<td>Pin and pad to Not be Populated</td>
</tr>
</tbody>
</table>

### H.110 TDM Bus (Computer Telephony)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CT_Dxx</td>
<td>H.110 TDM bus signals (8Mfps)</td>
</tr>
<tr>
<td>CT_C8A</td>
<td>8.192 MHz data clock</td>
</tr>
<tr>
<td>CT_C8_B</td>
<td>Redundant 8.192 MHz data clock</td>
</tr>
<tr>
<td>CT_FRAME_A</td>
<td>kHz frame clock</td>
</tr>
<tr>
<td>CT_FRAME_B</td>
<td>Redundant 8kHz frame clock</td>
</tr>
<tr>
<td>CT_NETREF_1</td>
<td>8kHz, 1.544MHz or 2.048MHz telecom network timing reference</td>
</tr>
<tr>
<td>CT_NETREF_2</td>
<td>Secondary 8kHz, 1.544MHz or 2.048MHz telecom network timing reference</td>
</tr>
<tr>
<td>CT_MC</td>
<td>2Mbps message channel</td>
</tr>
<tr>
<td>FR_COMP_</td>
<td>8kHz SCbus compatibility frame clock</td>
</tr>
<tr>
<td>SCLK</td>
<td>8.192MHz SCbus compatibility data clock</td>
</tr>
<tr>
<td>SCLKx2</td>
<td>Skewed 8.192MHz SCbus compatibility data clock</td>
</tr>
<tr>
<td>CT_EN_</td>
<td>Logical equivalent of the CPCI signal BD_SEL_ on P1</td>
</tr>
<tr>
<td>CT_Reset</td>
<td>Reset for use by CT Front Cards that do not populate P1</td>
</tr>
</tbody>
</table>
### Appendix 1 - Technical Reference

<table>
<thead>
<tr>
<th><strong>Telecom Power Bus</strong></th>
<th><strong>Telecom Ringing Bus</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>-Vbat</td>
<td>VRG</td>
</tr>
<tr>
<td>VbatRtn</td>
<td>VRGRtn</td>
</tr>
<tr>
<td>-SELVbat</td>
<td></td>
</tr>
<tr>
<td>SELVbatRtn</td>
<td></td>
</tr>
</tbody>
</table>

- **Telecom power source**
- **Telecom power source return**
- Short loop battery (voltage within SELV limits)
- Short loop battery return (voltage within SELV limits)
- Bussed ringing voltage
- Bussed ringing voltage return for VRG
Appendix 1 - Technical Reference

Backplane Slot Address Settings

<table>
<thead>
<tr>
<th>Physical Slot / Shelf Number</th>
<th>Pins 1,2</th>
<th>Pins 3,4</th>
<th>Pins 5,6</th>
<th>Pins 7,8</th>
<th>Pins 9,10</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Shorted</td>
<td>Shorted</td>
<td>Shorted</td>
<td>Shorted</td>
<td>Open</td>
</tr>
<tr>
<td>2</td>
<td>Shorted</td>
<td>Shorted</td>
<td>Shorted</td>
<td>Open</td>
<td>Shorted</td>
</tr>
<tr>
<td>3</td>
<td>Shorted</td>
<td>Shorted</td>
<td>Shorted</td>
<td>Open</td>
<td>Open</td>
</tr>
<tr>
<td>4</td>
<td>Shorted</td>
<td>Shorted</td>
<td>Open</td>
<td>Shorted</td>
<td>Shorted</td>
</tr>
<tr>
<td>5</td>
<td>Shorted</td>
<td>Shorted</td>
<td>Open</td>
<td>Shorted</td>
<td>Open</td>
</tr>
<tr>
<td>6</td>
<td>Shorted</td>
<td>Shorted</td>
<td>Open</td>
<td>Open</td>
<td>Shorted</td>
</tr>
<tr>
<td>7</td>
<td>Shorted</td>
<td>Shorted</td>
<td>Open</td>
<td>Open</td>
<td>Open</td>
</tr>
</tbody>
</table>

Table A1-6: Geographic and Shelf Address Settings

Jumper Definitions, 7-Slot Board

<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>System board in Slot 7 (CLK0-6 generated)</th>
</tr>
</thead>
<tbody>
<tr>
<td>JP10</td>
<td>2 &amp; 3 shorted</td>
</tr>
<tr>
<td>JP16</td>
<td>2 &amp; 3 shorted</td>
</tr>
<tr>
<td>JP20</td>
<td>This jumper controls local +12V sensing from the ATX connectors to the +12V plane. Shunting this jumper removes interoperability with PC-ATX power supplies and allows power supply backplanes to sense the +12V plane.</td>
</tr>
<tr>
<td>JP9</td>
<td>This 2-pin jumper controls the pushbutton reset function defined in the CompactPCI specification. When open the pushbutton reset signal floats. When shorted, the pushbutton reset signal is grounded.</td>
</tr>
</tbody>
</table>

Table A1-7: Jumper Definitions, 7-Slot Board
Appendix 1 - Technical Reference

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Appendix 2 - Glossary of Terms

B

backplane: A device inside the chassis that contains slots, or sockets, for plugging in cards or cables.

bidirectional parallel port: An eight-bit port that can be used for an input as well as an output device.

bus: One or more electrical conductors that transmit power or binary data to the various sections of a computer or any common pathway between hardware devices. A computer bus connects the CPU to its main memory and the memory banks that reside on the control units of the peripheral devices. It is made up of two parts. Addresses are sent over the address bus to signal a memory location, and the data are transferred over the data bus to that location.

C

card cage: A cabinet or metal frame that holds printed circuit cards.

CMOS (Complementary Metal Oxide Semiconductor): A technique of arranging transistors which uses very low power.

D

disk access LED: The LED located on the front control panel that indicates when the hard disk drive is active.

DRAM (Dynamic Random Access Memory): The main memory in your computer. It needs to be refreshed by a memory controller or it loses its information.

drive bay: Area in the chassis where drives are mounted.

E

electrostatic discharge (ESD): Stationary electrical charges in which no current flows. ESD can be prevented by wearing a wrist strap attached to a ground post on a static mat.
Appendix 2 - Glossary of Terms

EMI (ElectroMagnetic Interference): Noise generated by the switching action of the power supply and other system components. Conducted EMI is interference generally conducted into the power line, and is normally controlled with a line filter. Radiated EMI is that portion that radiates into free space. One way to suppress it is by enclosing circuitry in a metal case.

EPROM (Erasable Programmable Read Only Memory): A programmable device which stores information regardless of power.

expansion card: A printed circuit board that plugs into an expansion slot.

F

floppy drive: A device for reading the information contained on external, portable computer disks called floppy disks.

front control panel: The small panel on the front of the computer that contains the power switch, reset switch, Power ON LED, the disk access LED, and the keyboard connector.

H

hard drive: A data storage device. Hard drives magnetically store computer data on spinning internal disks.

hold-down bar: A metal bar located in the I/O bay of the chassis. It is used to keep I/O cards firmly seated in their slots. (There is no hold-down bar in CompactPCI systems.)

I

IDE (Integrated Drive Electronics): A standard of signalling and communicating with a device.

I/O card: A printed circuit board that plugs into an I/O slot.

I/O slot: A slot for plugging in additional I/O cards to expand the capability of a computer.
Appendix 2 - Glossary of Terms

ISA: The original IBM/PC clone plug-in board standard.

K

keyboard connector: The five-pin connector located on the front control panel.

kilobyte (KB): 1,024 bytes.

L

LED: Light Emitting Diode. Long-lasting light emitters usually used as indicators.

load board: A board having specific resistance to current flow.

P

parallel port: I/O connector used to hook up a printer or other parallel interface device. The parallel port is usually a 25-pin female DB25 connector.

PCI(Peripheral Component Interconnect): An optional slot standard for plug-in boards

port: Ports are used to connect peripheral devices such as external drives and printers to your computer.

power good: Signal used to prevent the computer from starting until the power has stabilized. The power good line switches from 0 to +5 volts within one tenth to one half second after the power supply reaches normal voltage levels. Whenever low input voltage causes the output voltage to fall below operating levels, the power good signal goes back to zero.

power ON/diagnostic LED: The LED located on the front control panel that indicates that power is present in the computer.

power supply: Electrical system that converts AC current from the wall outlet into the DC currents required by the computer circuitry. In a personal computer, +5, -5, +12 and -12 voltages are generated.
Appendix 2 - Glossary of Terms

**power switch**: Located on the front control panel, the power switch turns power ON to the computer.

**RAID (Redundant Array of Independent Disks)**: A storage technology using an array of two or more disks to redundantly store information. If one disk fails in a RAID array, the unit continues to function without loss of data.

**RAM (Random Access Memory)**: The memory used to execute applications while your computer is turned ON. When you turn your computer OFF, all data stored in RAM is lost.

**real-time clock (RTC)**: A periodic interrupt used to derive local time.

**reset switch**: Button or key that reboots the computer. All current activities are stopped cold and any data in memory are lost.

**retaining bracket**: The bracket on the back of the chassis that holds connectors from the board, usually a DB9 for serial port, a DB25 for parallel port, and mini-DIN connectors for keyboard and mouse.

**SCSI (Small Computer System Interface)**: A high speed, general purpose interface to storage devices.

**serial port**: A two-channel port, one channel used for "In" transmissions and one for "Out" transmissions.

**watchdog timer**: A device that watches for CPU inactivity and then resets the CPU after a specified duration of inactivity.
LIMITED WARRANTY

I-Bus/Phoenix warrants this product to be free of defects in material and workmanship for an initial period of two (2) years from date of delivery to the original purchaser from I-Bus/Phoenix.

During this period, I-Bus/Phoenix will, at its option, repair or replace this product at no additional charge to the purchaser, except as set forth in this warranty agreement.

I-Bus/Phoenix will, at its option, repair or replace this product at no additional charge to the purchaser, if the defect is related to the I-Bus/Phoenix manufactured product, such as power supply, backplanes, other chassis components, or CPUs. I-Bus/Phoenix is not liable for any defects in material or workmanship of any peripherals, products or parts which I-Bus/Phoenix does not design or manufacture. However, I-Bus/Phoenix will honor the original manufacturer’s warranty for these products.

I-Bus/Phoenix will analyze the defective component and the customer will be charged in the following instances:

- No problem found: $75 (U.S. dollars).
- Damage: parts and labor at $75 per hour with a $100 minimum charge (U.S. dollars). Receipt of damaged goods voids the I-Bus/Phoenix warranty.

Repair parts and replacement products will be furnished on an exchange basis and will be either new or reconditioned. All replacement parts and products shall become the property of I-Bus/Phoenix, if such parts or products are provided under this warranty agreement. In the event a defect is not related to the I-Bus/Phoenix manufactured product, I-Bus/Phoenix shall repair or replace the defective parts at purchaser’s cost and deliver the defective parts to the purchaser.

This Limited Warranty shall not apply if the product has been misused, carelessly handled, defaced, modified or altered, or if unauthorized repairs have been attempted by others.

The above warranty is the only warranty authorized by I-Bus/Phoenix and is in lieu of any implied warranties, including implied warranty of merchantability and fitness for a particular purpose.

In no event will I-Bus/Phoenix be liable for any such damage as lost business, lost profits, lost savings, downtime or delay, labor, repair or material cost, injury to person or property or any similar or dissimilar consequential loss or damage incurred by purchaser, even if I-Bus/Phoenix has been advised of the possibility of such losses or damages.

In order to obtain warranty service, the product must be delivered to the I-Bus/Phoenix facility, or to an authorized I-Bus/Phoenix service representative, with all included parts and accessories as originally shipped, along with proof of purchase and a Returned Merchandise Authorization (RMA) number.

The RMA number is obtained, in advance, from I-Bus/Phoenix Customer Service Department and is valid for 30 days. The RMA number must be clearly marked on the exterior of the original shipping container or equivalent. Purchaser will be responsible and liable for any missing or damaged parts. Purchaser agrees to pay shipping charges one way, and to either insure the product or assume the liability for loss or damage during transit. Ship to:

I-Bus/Phoenix

ATTENTION: RMA REPAIR DEPT.

RMA ####

8888 Balboa Avenue
San Diego, CA 92123
Appendix 3 - Limited Warranty

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Appendix 4 - FCC Information

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received including interference that may cause undesired operation.

WARNING: This equipment has been tested and found to comply with the limits for a Class “A” digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at their own expense.

Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

NOTE: This product was FCC verified under test conditions that included the use of shielded I/O cables and connectors between system components. To be in compliance with FCC regulations, the user must use shielded cables and connectors and install them properly.
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